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(54) Semiconductor memory devices.

(57) A semiconductor memory device, that has a plurality of writing ports (WP_0, WP_1) and reading ports (RP_0 to RP_3) comprises a first data latch portion (11 ; 111 ; 211), at least one second data latch portion (12 to 1k ; 12 to 14 ; 112 to 11k ; 212, 213), and communication units (41 to 4k, 5 ; 41 to 44, 51 to 54, 221, 222a, 222b, 223). The first data latch portion (11 ; 111 ; 211) is directly accessible by externally entering an address signal, and the second data latch portions (12 to 1k ; 12 to 14 ; 112 to 11k ; 212, 213) are connected in parallel to the first data latch portion (11 ; 111 ; 211). The communication units (41 to 4k, 5 ; 41 to 44, 51 to 54, 221, 222a, 222b, 223) is used to access one of the first and second data latch portions (11 to 1k ; 11 to 14 ; 111 to 11k ; 211 to 213).

Such a semiconductor memory device is applicable to a register file of a microprocessor, for example, and involves a reduced amount of hardware in the register file, particularly in the case of a processor employing parallel processing and local register architecture.

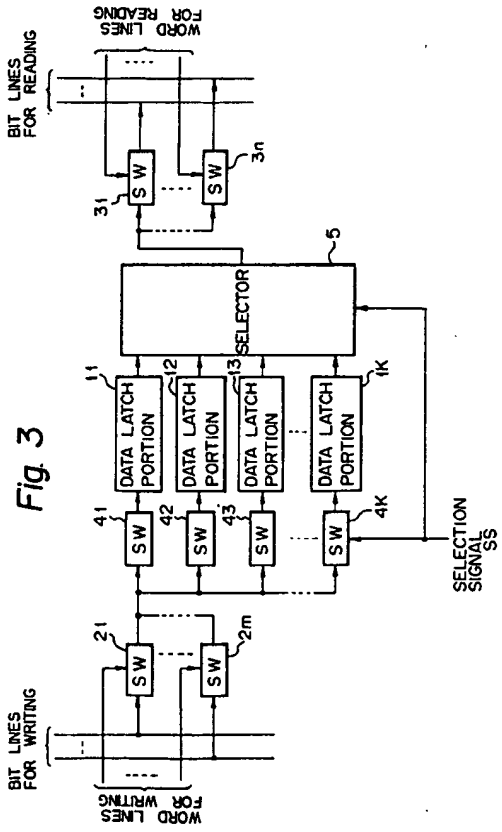

Fig. 3

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The present invention relates to semiconductor memory devices and, more particularly, to semiconductor memory devices having a plurality of writing ports and reading ports.

Recently, microprocessors (arithmetic processing devices, or processors) generally comprise an instruction fetching unit, instruction decoding unit, arithmetic operation executing unit, register file, and the like. Further, these microprocessors have been, for example, designed to execute instructions by pipeline operation.

A previously-considered microprocessor includes only one arithmetic operation executing unit, and thus the register file may comprise a semiconductor memory device (for example, SRAM) having two-read/one-write ports. Such semiconductor memory devices having two-read/one-write ports can effectively carry out three address type arithmetic operations, such as adding instructions.

Some microprocessors employ parallel processing architecture, such as VLIW (Very Long Instruction Word) or Superscaler, and the like, to enable higher speed processing. Microprocessors employing such types of architecture may include a plurality of arithmetic operation executing units and semiconductor memory devices having a plurality of read/write ports for performing a transfer of data between a plurality of arithmetic operation executing units and semiconductor memory devices (register file).

In general, for n number of arithmetic operation execution units, 2n reading ports and n writing ports need to be provided by the semiconductor memory devices. Incidentally, in order to execute a sub-routine call or other such instruction, a microprocessor architecture having a plurality of local register files has been considered.

However, such an architecture requires a large number of local register files since it assigns a specific local register file for each sub-routine. Such type of register file may, for example, be formed by employing a plurality of two-read/one-write ports semiconductor memory devices.

On the other hand, in accordance with the progress of semiconductor technology, data processing devices capable of high speed performance have been developed, and arithmetic processing devices (microprocessors) that are capable of performing parallel arithmetic operations have been provided. Accordingly, semiconductor memory devices (for example, multi-port SRAM) having a plurality of writing ports and reading ports have been developed. However, these semiconductor memory devices have a large amount of hardware, and they are expensive.

Various aspects of the invention are exemplified by the attached claims.

It will be apparent that it is thus possible to provide a semiconductor memory device having a plurality of writing ports and reading ports which requires a small amount of hardware and is inexpensive.

An embodiment of the present invention can provide a semiconductor memory device having a plurality of writing ports and reading ports for carrying out parallel writing and reading operations through the writing ports and the reading ports, wherein the semiconductor memory device comprises: a first data latch portion directly accessible by externally entering an address signal; at least one second data latch portions parallel connecting to the first data latch portion; and a communication unit for accessing one of the first-and second data latch portions.

The writing ports may be operatively connected to the first and second data latch portions through writing control transfer gates, and the reading ports may be operatively connected to the first and second data latch portions through reading control transfer gates. The communication unit may comprise a plurality of data latch portion selecting transfer gates provided at a respective writing side and reading side relative to the first and second data latch portions parallel connected, for selecting one of the first and second data latch portions in accordance with a selection signal.

The selection signal may be dependently generated by using a selection register, or it may be generated by using a selection signal decoder receiving a part of the address signal.

The writing data may be transferred from the writing ports to one of the first and second data latch portions through a plurality of bit lines for writing, and reading data may be transferred from one of the first and second data latch portions to reading ports through a plurality of bit lines for reading. The connection between the bit lines for writing and the first and second data latch portions may be controlled by a plurality of writing port selection gates, and the connection between the first and second data latch portions and the bit lines for reading may be controlled by a plurality of reading port selection gates.

The writing ports may be operatively connected to the first data latch portion through writing control transfer gates, and the reading ports may be operatively connected to the first data latch portion through reading control transfer gates. The communication unit may comprise a plurality of shifting control transfer gates for shifting data of one of the second data latch portions to the first data latch portion and for accessing one of the first and second data latch portions in accordance with a control signal. The control signal may be determined to an externally supplied clock signal.

The writing data may be written from the writing ports into the first data latch portion through a plurality of bit lines for writing, reading data may be read out from the first latch portion to reading ports through a plurality of bit lines for reading, and the data stored in the first data latch portion may be shifted to the sec-

ond data latch portions. The connection between the bit lines for writing and the first data latch portions may be controlled by a plurality of writing port selection gates, and the connection between the first data latch portions and the bit lines for reading may be controlled by a plurality of reading port selection gates.

A further embodiment of the present invention can provide an arithmetic processing device formed by one chip configuration having an instruction fetching unit for fetching an instruction, an instruction decoding unit for decoding the instruction fetched in the instruction fetching unit, a plurality of arithmetic operation executing units for carrying out arithmetic operations in parallel, and a register file for storing data having a plurality of writing ports and reading ports to carry out writing and reading operations in parallel through the writing ports and the reading ports, wherein the register file comprises: a first data latch portion directly accessible by externally entering an address signal; at least one second data latch portions parallel connecting to the first data latch portion; and a communication unit for accessing one of the first and second data latch portions.

Reference will now be made, by way of example, to the accompanying drawings, in which:

Figures 1A and 1B are block diagrams showing an example of a previously-considered semiconductor memory device;

Figure 2 is a circuit diagram of a part of a SRAM having four-read/two-write ports to which the semiconductor memory device of Figs. 1A and 1B has been applied;

Figure 3 is a block diagram showing parts of a semiconductor memory device according to a first embodiment of the present invention;

Figure 4 is a circuit diagram of a part of a SRAM having four-read/two-write ports, to which the semiconductor memory device of Fig. 3 has been applied;

Figure 5 is a circuit diagram showing in greater detail four SRAM cells included in the SRAM of Fig. 4;

Figure 6 is a block diagram of a semiconductor memory device embodying the present invention;

Figure 7 is a block diagram showing an example of a selection signal generation circuit included in the Fig. 6 device;

Figure 8 is a block diagram showing another example of the selection signal generation circuit;

Figure 9 is a block diagram of parts of a microprocessor employing two arithmetic operation execution units and a semiconductor memory device embodying the present invention;

Figure 10 is a block diagram showing parts of a semiconductor memory device according to a second embodiment of the present invention; and

Figures 11A and 11B are block diagrams showing a practical implementation of the Fig. 10 semiconductor memory device.

Figures 1A and 1B show a semiconductor memory device which has a plurality of read/write ports (n-read/m-write ports) and is provided with m write selection switch units (writing port selection gates) 321 to 32m, and n read selection switch units (reading port selection gates) 331 to 33n for one data latch portion (memory cell) 311. Note, as shown in Fig. 1A, each of the writing port selection gates 321 to 32m is provided at an intersectional portion between one of the bit lines for writing (writing bit lines) and one of the word lines for writing (writing word lines). Similarly, each of the reading port selection gates 331 to 33n is provided at an intersectional portion between one of the bit lines for reading (reading bit lines) and one of the word lines for reading (reading word lines). Therefore, the number of writing bit lines and writing word lines is the same as the number (m) of writing port selection gates 321 to 32m, and the number of reading bit lines and reading word lines is the same as the number (n) of reading port selection gates 331 to 33n.

As shown in Fig. 1B, the register file has k memory devices (n-read/m-write memories) 301 to 30k and is designed to be selected by a selector 305. The register file of a microprocessor (arithmetic processing devices, or processors) employing parallel processing architecture and local register type (number of local register is generally referred to as k) may be consitituted by k sets of n-read/m-write memories having m writing ports and n reading ports.

Figure 2 shows a part of a SRAM having four-read/two-write ports to which the semiconductor memory device of Figs. 1A and 1B is applied. In Fig. 2, references BL_0 and BL_1 denote bit lines for writing (writing bit lines), WL_0 and WL_1 denote word lines for writing (writing word lines), BL_2, to BL_5 denote bit lines for reading (reading bit lines), and WL_2 to WL_5 denote word lines for reading (reading word lines).

As shown in Fig. 2, the SRAM having four-read/two-write ports has the construction in which two writing port selection gates 321 and 322 and four reading port selection gates 331 to 334 are provided for each SRAM cell 311. Further, each of the writing port selection gates 321 and 322 is provided at an intersectional portion between one of the writing bit lines BL_0 and BL_1 and one of the writing word lines WL_0 and WL_1. Similarly, each of the reading port selection gates 331 to 334 is provided at an intersectional portion between one of the reading bit lines BL_2 to BL_5 and one of the reading word lines WL_2 to WL_5.

Note, the two writing ports (WP_0, WP_1) are operatively connected to the writing bit lines BL_0 and BL_1 through a sense amplifier, and the like, to write data into each of the SRAM cells 311. Similarly, the four reading ports (RP_0, RP_1, RP_2, RP_3) are operatively connected to the reading bit lines BL_2 to BL_5 through the sense amplifier, and the like, to read out data from each of the SRAM cells 311. Further, in a micropro-

cessor including the semiconductor memory device, the writing ports WP_0, WP_1 and reading ports RP_0 to RP_3 are not external ports of the microprocessor, but are connected internally of the microprocessor to arithmetic operation executing units (for example, ALUs: Arithmetic and Logic Units) provided in the microprocessor to internally transfer data between the arithmetic operation executing units and the semiconductor memory device (register file).

As described above, a semiconductor memory device having a plurality of read/write ports as illustrated in Fig. 1A and-1B is constituted of k local registers (n-read/m-write memories) having m writing ports and n reading ports and thus requires a hardware amount of ((n-read/m-write memories) × k + selector). Accordingly, multi-port semiconductor memory devices, and microprocessors including such devices, are indesirably expensive.

In more detail, in the SRAM shown in Fig. 2 having four-read/two-write ports, two writing ports WP_0, WP_1 (writing bit lines BL_0, BL_1) are connected to the SRAM cell 311 (one memory cell) through two writing port selection gates 321 and 322, and four reading ports RP_0 to RP_3 (reading bit lines BL_2 to BL_5) are connected to the SRAM cell 311 through four reading port selection gates 331 to 334. Accordingly, in this case, six transistors (transfer gates 321, 322; 331, 332, 333, 334) are needed for one memory cell (SRAM cell 311). Consequently, the hardware amount required for a large number of memory cells (311) becomes substantial.

The semiconductor memory device of Fig. 3 has a plurality of read/write ports (n-read/m-write) and comprises m write selection switch units (writing port selection gates) 21 to 2m and n read selection switch units (reading port selection gates) 31 to 3n for a plurality of (k) data latch portions (memory cells) 11 to 1k.

As shown in Fig. 3, the semiconductor memory device has a first data latch portion 11 directly accessible by externally entering the address, and second data latch portions 12 to 1k provided parallel to the first data latch portion 11. The first and each of the second data latch portions 11 to 1k are provided with respective switching units (data latch portion selecting transfer gates) 41 to 4k and a selector 5. For each of the switching units 41 to 4k and the selector 5, a selection signal SS is supplied to selectively access one of the first and second data latch portions 11 to 1k.

Note, in this embodiment, since one of the first and second data latch portions 11 to 1k can be selected by the selection signal SS, the content of the directly accessible memory cell by externally entering an address can be replaced depending upon the designation of the local register file. Namely, by assigning the local register file for respective data latch portions 11 to 1k, one of the targeted data latch portions can be exclusively selected by the switching units 41 to 4k according to the progress of the program.

Figure 4 shows a part of a SRAM having four-read/two-write ports, to which the semiconductor memory device of Fig. 3 is applied, and further, Fig. 5 shows the configuration of four SRAM cells of Fig. 4.

In Figs. 4 and 5, references BL_0 and BL_1 denote bit lines for writing (writing bit lines), WL_0 and WL_1 denote word lines for writing (writing word lines), BL_2 to BL_5 denote bit lines for reading (reading bit lines), and WL_2 to WL_5 denote word lines for reading (reading word lines).

As shown in Fig. 4, the SRAM has two writing port selection gates 21, 22 and four reading port selection gates 31 to 34 for four SRAM cells 11 to 14. Namely, as shown in Fig. 4, each of the writing port selection gates 21 and 22 is provided at an intersectional portion between one of the writing bit lines BL_0 and BL_1 and one of the writing word lines WL_0 and WL_1. Similarly, each of the reading port selection gates 31 to 34 is provided at an intersectional portion between one of the reading bit lines BL_2 to BL_5 and one of the reading word lines WL_2 to WL_5. Further, each SRAM 11 to 14 is provided with data latch portion selecting transfer gates 41 to 44 at the writing side and data latch portion selecting transfer gates 51 to 54 at the reading side. These data latch portion selecting transfer gates 41 to 44 and 51 to 54 are controlled by the selection signal SS, so that one of the desired SRAM cells can be selected.

Note, the two writing ports (WP_0, WP_1) are operatively connected to the writing bit lines BL_0 and BL_1 through a sense amplifier, and the like, to write data into one of the selected SRAM cells 11 to 14. Similarly, the four reading ports (RP_0, RP_1, RP_2, RP_3) are operatively connected to the reading bit lines BL_2, to BL_5 through the sense amplifier, and the like, to read out data from one of the selected SRAM cells 11 to 14. Further, in a microprocessor including the semiconductor memory device, the writing ports WP_0, WP_1 and reading ports RP_0, to RP_3 are not external ports of the microprocessor, but are connected to arithmetic operation execution units (for example, ALUs: Arithmetic and Logic Units) provided in the microprocessor to internally transfer data between the arithmetic operation execution units and the semiconductor memory device (register file).

By comparing the SRAM shown in Fig. 4 with that of Fig. 2, the present embodiment of a SRAM having four-read/two-write ports of Fig. 4 requires fourteen transistors (transfer gates 21, 22; 31, 32, 33, 34; 41, 42, 43, 44; 51, 52, 53, 54) for four memory cells (SRAM cells) 11, 12, 13 14, however, the SRAM having four-read/two-write ports of Fig. 2 requires six transistors (transfer gates 321, 322; 331, 332, 333, 334) for one memory cell (SRAM cell) 311. Namely, in the present embodiment shown in Fig. 4, only 3.5 (14/4) transistors are required per memory cell, and thus can reduce the hardware amount involved in an

SRAM having the same capacity.

Figure 6 shows a complete semiconductor memory device embodying the present invention. In Fig. 6, reference numeral 100 denotes a selection register, 200 denotes a row address decoder, and 300 denotes a column address decoder and sense amplifier. As shown in Fig. 6, an address signal (address signals) is supplied to the row address decoder 200 and the column address decoder and sense amplifier 300. Note, as shown in Fig. 6, the two writing ports WP_0, WP_1 are connected to the memory cells (data latch portions) through sense amplifiers, the writing bit lines BL_0 and BL_1, and the like. Similarly, the four reading ports RP_0, RP_1, RP_2, RP_3 are connected to the memory cells through the sense amplifiers, the reading bit lines BL_2 to BL_5, and the like.

The selection register 100 receives selection data and stores the selection data into a register provided in the selection register 100, and further the selection register 100 outputs a selection signal SS to a memory cell array. Namely, the selection signal SS is supplied to the data latch portion selecting transfer gates (41 to 4k and 51 to 54) to selectively access one of the desired first and second data latch portions (11 to 1k.)

Figure 7 shows an example of a selection signal generation circuit. In Fig. 7, reference numerals 621 to 624 denote selectors, 631 to 634 denote registers, and 61 denotes an AND gate.

As shown in Fig. 7, a shift enabling signal SE is supplied to one input terminal of the AND gate 61 and a clock signal CLK is inverted and supplied to another input terminal of the AND gate 61, and an output signal of the AND gate 61 is supplied to the registers 631 to 634. Further, a shift control signal SCS is supplied to the selectors 621 to 624, an output signal of each of the selectors 621 to 624 is supplied to the corresponding registers 631 to 634, and an output signal of each of the registers 631, 632, 633, 634 is supplied to the adjacent selectors 622, 623, 624, 621.

Further, as shown in Fig. 7, the selector 621 is constituted by two AND gates 6211 and 6212 and an OR gate 6213. In the selector 621, the output signal (Q-output signal) of the register 632 is input to one input terminal (S1) of the AND gate 6211, and the shift control signal SCS is inverted and input to another input terminal of the AND gate 6211. Similarly, the output signal (Q-output signal) of the register 634 is input to one input terminal (S2) of the AND gate 6212, and the shift control signal SCS is directly input to another input terminal of the AND gate 6212. Further, output signals of the AND gates 6211 and 6212 are input to input terminals of the OR gate 6213. Note, each of the selectors 622 to 624 is constituted similarly to the selector 621.

Note, this selection signal generation circuit of Fig. 7 is used to generate four selection signals SS (SS_1 to SS_4) for selecting the data latch portion selecting transfer gates 41 to 44 and 51 to 54 shown in Figs. 4 and 5. Namely, for example, a first selection signal SS, is supplied to the gates of the transistors (data latch portion selecting transfer gates) 41 and 51 for a first SRAM cell (memory cell) 11, a second selection signal SS, is supplied to the gates of the transistors 42 and 52 for a second SRAM cell 12, a third selection signal SS, is supplied to the gates of the transistors 43 and 53 for a third SRAM cell 13, and a fourth selection signal SS_4 is supplied to the gates of the transistors 44 and 54 for a fourth SRAM cell 14.

In this case, when the shift enabling signal SE is at a high level "H", the selection signals SS_1 to SS_4 are shifted, that is the selection signals SS_1 to SS_4 are output in a sequential fashion. Namely, the SRAM cells 11 to 14 are selected sequentially and accessed. Conversely, when the shift-enabling signal SE is at a low level "L", the selection signals SS, to SS_4 are not shifted.

Note, in the case that the shift enabling signal SE is at the high level "H", and when the shift control signal SCS is at a high level "H", the selection signals SS_1 to SS_4 are shifted in clockwise rotation, so that the four SRAM cells 11 to 14 are accessed in an orderly manner. Namely, the SRAM cells 11 to 14 of Fig. 4 are selected as $11 \rightarrow 12 \rightarrow 13 \rightarrow 14 \rightarrow 11 \rightarrow \cdots$, in accordance with the clock signal CLK. Conversely, in the case that the shift enabling signal SE is at the high level "H", and when the shift control signal SCS is at a low level "L", the SRAM cells 11 to 14 of Fig. 4 are selected as $11 \rightarrow 14 \rightarrow 13 \rightarrow 12 \rightarrow 11 \rightarrow \cdots$, in accordance with the clock signal CLK.

Figure 8 is a block diagram showing another example of a selection signal generation circuit. In Fig. 8, a reference numeral 400 denotes a selection signal decoder. Note, the selection signal generation circuit shown in Fig. 8 generates the selection signal SS by using address signals (AD0 and AD1); however, the selection signal generation circuit shown in Fig. 7 generates the selection signal SS by using the shift enabling signal SE, the shift control signal SCS, and the clock signal CLK.

For example, as shown in Fig. 8, j-bits of the address signals AD0 to ADj supplied to the semiconductor memory device consist of two components AD0, AD1 and AD2 to ADj. One component the address signals AD0 and AD1) is used to generate the selection signal SS (for example, four selection signals SS_1 to SS_4), and the other component of the address signals (AD2 to ADj), which corresponds to normal address signals, is used to select and access a specific memory cell in the memory cell array. Namely, as shown in Fig. 8, two bits of the address signals AD0 and AD1 are supplied to a selection signal decoder 400; the address signals AD0 and AD1 are decoded by the selection signal decoder 400, and four selection signals SS_1 to SS_4 are generated and supplied to the register file 1.

Figure 9 is a block diagram showing an example

of a microprocessor employing two arithmetic operation execution units and a semiconductor memory device embodying the present invention. In Fig. 9, reference numeral 1 denotes a register file (semiconductor memory device); 2 and 3 denote ALUs (arithmetic operation execution units); 100 denotes a selection register, 101 denotes an instruction decoding unit, and 102 denotes an instruction fetching unit. Note, in this example, two ALUs 2 and 1 are provided, and thus the register file 1 is constituted of a four-read/two-write memory (SRAM having four-read/two-write ports).

The microprocessor (arithmetic processing device), which is formed by one chip configuration, comprises the instruction fetching unit 102, the instruction decoding unit 101, the register file 1, and two ALUs 2, 3. The instruction fetching unit 102 is used to fetch an instruction, and the instruction decoding unit 101 is used to decode the instruction fetched in the instruction fetching unit 102. The register file 1 is used to store data, and the ALUs are used to carry out parallel arithmetic operations. Note, as described above, the register file (semiconductor memory device) 1 includes a plurality of data latch portions 11 to 14, and selectors 51 to 54 (corresponding to selector 5).

As shown in Fig. 9, the ALU 2 is connected to the register file 1 by one writing port WP_0 (writing bit line BL_0) and two reading ports RP_0 and RP_1 (reading bit lines BL_2 and BL_3), and similarly, the ALU 3 is connected to the register file 1 by one writing port WP_1 (writing bit line BL_1) and two reading ports RP_2 and RP_3 (reading bit lines BL_4 and BL_5). Namely, two data are read out from the register file 1 to the ALU 2, and another two data can be read out from the register file 1 to the ALU 3 at the same time. Further, the results of an arithmetic operation of the ALUs 2 and 3 are again stored in the register file 1. Therefore, two arithmetic operations can be carried out by two ALUs 2 and 3 in parallel formation.

Figure 10 shows another semiconductor memory device embodying the present invention. Note, in the embodiment shown in Fig. 3, a plurality of data latch portions 11 to 1k are parallel connected and one of the data latch portions 11 to 1k is randomly selected by the selection signal SS. In contrast, in the embodiment shown in Fig. 10, a first data latch portion lll,directly accessible by externally entering an address,and a plurality of second data latch portions 112 to 11k provided in parallel formation relative to the first data latch portion 11L are directly connected by a communication unit (not shown) so that one of the first and second data latch portion 111 to 11k can be accessed by shifting the data in order (for example, clockwise shifting) with a clock signal CLK. Namely, for example, when data stored in the data latch portion 113 are read out, the data stored in the data latch portion 113 is shifted to the data latch portion 111 through the data latch portion 112 with two cycles of a clock signal CLK, and then the data shifted to the data latch portion 111 is read out. Note, for example, when writing specific data into the data latch portion 113 after writing the specific data at the data latch portion 111, the data is shifted to the data latch portion 113 in order by the clock signal CLK. Further, the second data latch portions (112 to 11k) may be determined to one.

In the above description, the data shift of the clockwise rotation denotes that data stored (latched) in the first SRAM cell 111 is transferred to the second SRAM cell 112, or data stored in the third SRAM cell 113 is transferred to the fourth SRAM cell 114 in response to one clock signal CLK..

Figures 11A and 11B show a practical embodiment of the semiconductor memory device of Fig. 10.

As shown in Fig. 11A, in the semiconductor memory device having a plurality of read/write ports (n-read/m-write ports), two data latch portions 212 and 213 are provided for one data latch portion (memory cell 211), and switching units (shifting control transfer gate) 221a, 221b, 222 and 223 are provided for directly connecting the data latch portions 211, 212 and 213. Note, as shown in Fig. 11A, each of the switching units 221a, 221b, 222 and 223 is, for example, constituted by an N-type MOS transistor, and each of the data latch portions 211, 212 and 213 is, for example, constituted by a D-type flip-flop.

Note, in the embodiment of Figs. 11A and 11B the data stored in each data latch portions 211, 212 and 213 are adapted to be both clockwise and counterclockwise shifted. Further, in this embodiment, three bit memory cells (data latch portion) are provided, but it will be appreciated that memory cells having k bits may be provided to shift the data, as required. Furthermore, the signal to control the shifting of data need not be the clock signal CLK supplied from an external semiconductor memory device

As shown in Fig. 11B, the register file is formed with only a n-read/m-write × k memory 500 having k number of memory cells. Namely, by applying this embodiment of Figs. 11A and 11B, a semiconductor memory device (n-read/m-write memory 301 to 30k) having the same capacity as that of Figs. 1A and 1B can be constituted of only the n-read/m-write × k memory 500, so that the hardware amount can be significantly reduced. Note, the semiconductor memory device can be separated into a memory cell array portion and a peripheral portion (decoder, buffer, selector, sense amplifier, and the like). However, in an embodiment of the present invention, when an increase in the number (k) of local register files is desired, only the size of a memory array depends on the number of local register files, and an increase of hardware amount relative to the number of the local register file can be made smaller than that in previously-considered devices (for example, less than or equal to 50% of the amount of hardware in such devices).

Consequently, in the semiconductor memory de-

vice shown in Figs. 11A and 11B, the amount of hardware of the register file of the microprocessor employing a parallel processing and local register architecture can be reduced. In particular, when a plurality of local register files are provided, the hardware amount can be reduced significantly.

As described above, in a semiconductor memory device embodying the present invention, the hardware amount of the register file of a microprocessor employing parallel processing and local register architecture can be significantly reduced by providing a first data latch portion and at least one second data latch portion having a communication unit and accessing one of the desired first and second data latch portions.

Claims

1. A semiconductor memory device comprising a plurality of writing ports (WP_0, WP_1) and a plurality of reading ports (RP_0, RP_3), characterised by a plurality of coupled data latches (11 to 1k, 112 to 11k, 211 to 213), each of the writing ports (WP_0, WP_1) being coupled to at least a first of the plurality of latches by a writing control device (21 to 2m, 121 to 12m) and each of the reading ports (RP_0 to RP_3) being coupled to at least the first of the plurality of latches by a reading control device (31 to 3n, 131 to 13n), at least one of said control devices being common to said plurality of latches and there being selection means (41 to 4k, 5, 51 to 54, 221, 222a, 222b, 223) for selecting that one of the latches to be accessed by the common reading and/or writing control device.

2. A semiconductor memory device according to claim 1, wherein said plurality of coupled data latches (11 to 1k, 112 to 11, 211 to 213) are coupled in parallel with each other.

3. A semiconductor memory device according claim 1, wherein said writing ports (WP_0, WP_1) and reading ports (RP_0, RP_3) are connected to a first of the data latches (11, 111, 211) by respective ones of the writing and reading control devices, and wherein the or each other latch (12 to 1k, 12 o 14, 112 to 11k, 212, 213) of the plurality of latches is accessed by the common reading and/or writing control device by shifting data through the latches.

4. A semiconductor memory device having a plurality of writing ports (WP_0, WP_1) and reading ports (RP_0 to RP_3) for carrying out parallel writing and reading operations through said writing ports (WP_0, WP_1) and said reading ports (RP_0 to RP_3), characterized in that said semiconductor memory device comprises:

a first data latch portion (11; 111; 211) directly accessible by externally entering an address signal (AD0 to ADj);

at least one second data latch portions (12 to 1k; 12 to 14; 112 to 11k; 212, 213) parallel connecting to said first data latch portion (11; 111; 211); and

a communication means (41 to 4k, 5; 41 to 44, 51 to 54; 221, 222a, 222b, 223) for accessing one of said first and second data latch portions (11 to 1k; 11 to 14; 111 to 11k; 211 to 213).

5. A semiconductor memory device as claimed in claim 4, wherein said writing ports (WP_0, WP_1) are operatively connected to said first and second data latch portions (11 to 1k; 11 to 14) through writing control transfer gates (21 to 2m; 21, 22), and said reading ports (RP_0 to RP_3) are operatively connected to said first and second data latch portions (11 to 1k; 11 to 14) through reading control transfer gates (31 to 3n; 31 to 14).

6. A semiconductor memory device as claimed in claims 4 or 5, wherein said communication means comprises a plurality of data latch portion selecting transfer gates (41 to 44; 41 to 4k: 51 to 54) provided at a respective writing side and reading side relative to said first and second data latch portions (11 to 1k; 11 to 14) parallel connected, for selecting one of said first and second data latch portions (11 to 1k; 11 to 14) in accordance with a selection signal (SS; SS_1 to SS_4).

7. A semiconductor memory device as claimed in claim 6, wherein said selection signal (SS; SS_1 to S_4) is dependently generated by using a selection register (100).

8. A semiconductor memory device as claimed in claim 7, wherein said selection signal (SS; SS_1 to SS_4) is generated by using a selection signal decoder (400) receiving a part (AD0, AD1) of said address signal (AD0 to ADj).

9. A semiconductor memory device as claimed in any one of the preceding claims, wherein writing data are transferred from said writing ports (WP_0, WP_1) to one of said first and second data latch portions (11 to 1k; 11 to 14) through a plurality of bit lines (BL_0, BL_1) for writing, and reading data are transferred from one of said first and second data latch portions (11 to 1k; 11 to 14) to reading ports (RP_0 to RP_3) through a plurality of bit lines (BL_2 to BL_5) for reading.

10. A semiconductor memory device as claimed in claim 9, wherein the connection between said bit

lines (BL_0, BL_1) for writing and said first and second data latch portions (11 to 1k; 11 to 14) are controlled by a plurality of writing port selection gates (21, 22; 21 to 2m), and the connection between said first and second data latch portions (11 to 1k; 11 to 14) and said bit lines (BL_2 to BL_5) for reading are controlled by a plurality of reading port selection gates (31 to 34; 31 to 3n).

11. A semiconductor memory device as claimed in claim 4, wherein said writing ports (WP_0, WP_1) are operatively connected to said first data latch portion (111; 211) through writing control transfer gates (121 to 12m), and said reading ports (RP_0 to RP_3) are operatively connected to said first data latch portion (111; 211) through reading control transfer gates (131 to 13n).

12. A semiconductor memory device as claimed in claim 11,wherein said communication means comprises a plurality of shifting control transfer gates (221, 222a, 222B, 223) for shifting data of one of said second data latch portions (212, 213) to said first data latch portion (211) and for accessing one of said first and second data latch portions (211 to 213) in accordance with a control signal.

13. A semiconductor memory device as claimed in claim 12, wherein said control signal is an externally supplied clock signal (CLK).

14. A semiconductor memory device as claimed in claim 11, wherein writing data are written from said writing ports (WP_0, WP_1) into said first data latch portion (111; 211) through a plurality of bit lines (BL_0, BL_1) for writing, reading data are read out from said first latch portion (111; 211) to reading ports (RP_0 to RP_3) through a plurality of bit lines (BL_2 to BL_5) for reading, and the data stored in said first data latch portion (111; 211) are shifted to said second data latch portions (112 to 11k; 212, 213).

15. A semiconductor memory device as claimed in claim 14, wherein the connection between said bit lines (BL_0, BL_1) for writing and said first data latch portions (111; 211) are controlled by a plurality of writing port selection gates (121 to 12m), and the connection between said first data latch portions (111; 211) and said bit lines (BL_2 to BL_5) for reading are controlled by a plurality of reading port selection gates (131 to 13n).

16. A semiconductor memory device as claimed in any one of the preceding claims, wherein said semiconductor memory device is applied to an arithmetic processing device as a register file (1), and said arithmetic processing device is formed by one chip configuration and has an instruction fetching unit (102) for fetching an instruction, an instruction decoding unit (101) for decoding said instruction fetched in said instruction fetching unit (102), a plurality of arithmetic operation executing units (2, 3) for carrying out parallel arithmetic operations.

17. A microprocessor having an arithmetic logic unit and, coupled thereto, a register with a semiconductor memory device according to any one of the preceding claims.

Fig. 1A

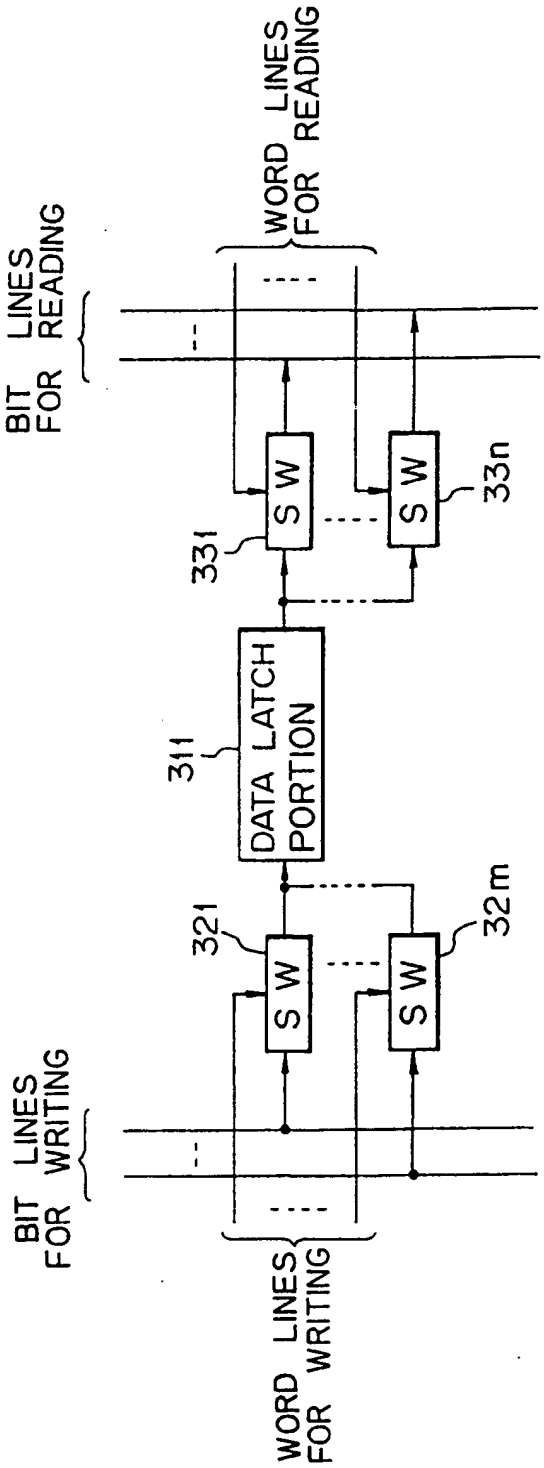
BIT LINES FOR READING
WORD LINES FOR READING
331
S W
33n
311
DATA LATCH PORTION
321
32m
BIT LINES FOR WRITING
WORD LINES FOR WRITING

Fig. 1B

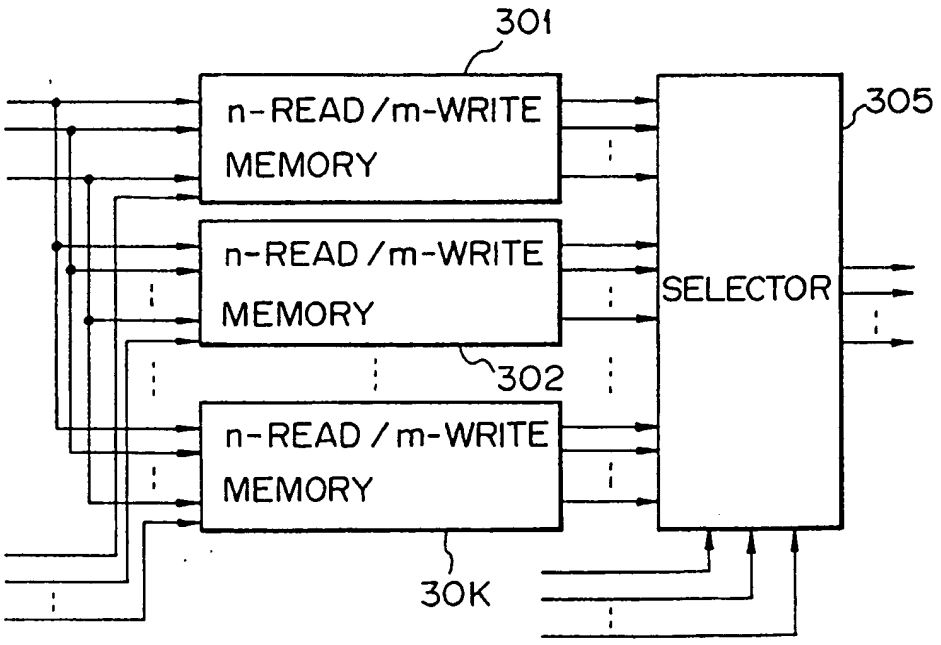
301
n-READ/m-WRITE MEMORY
n-READ/m-WRITE MEMORY
302
n-READ/m-WRITE MEMORY
30K
SELECTOR
305

Fig. 2

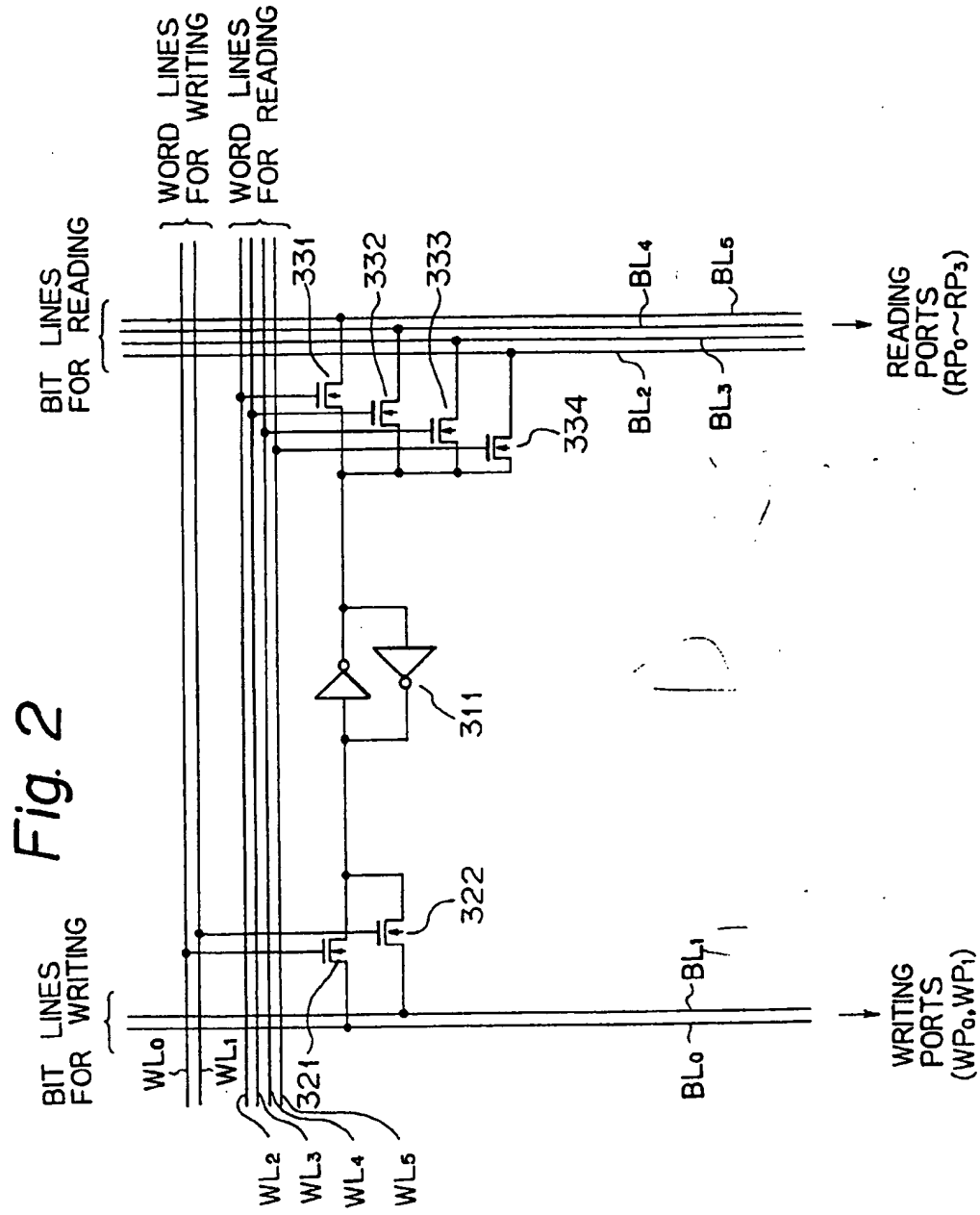
BIT LINES FOR READING
WORD LINES FOR WRITING
WORD LINES FOR READING
331
332
333
334
BL4
BL5
BL2
BL3
READING PORTS (RP0~RP3)
311
322
BL1
BIT LINES FOR WRITING
WL0
WL1
321
WL2
WL3
WL4
WL5
BL0
WRITING PORTS (WP0,WP1)

Fig. 3

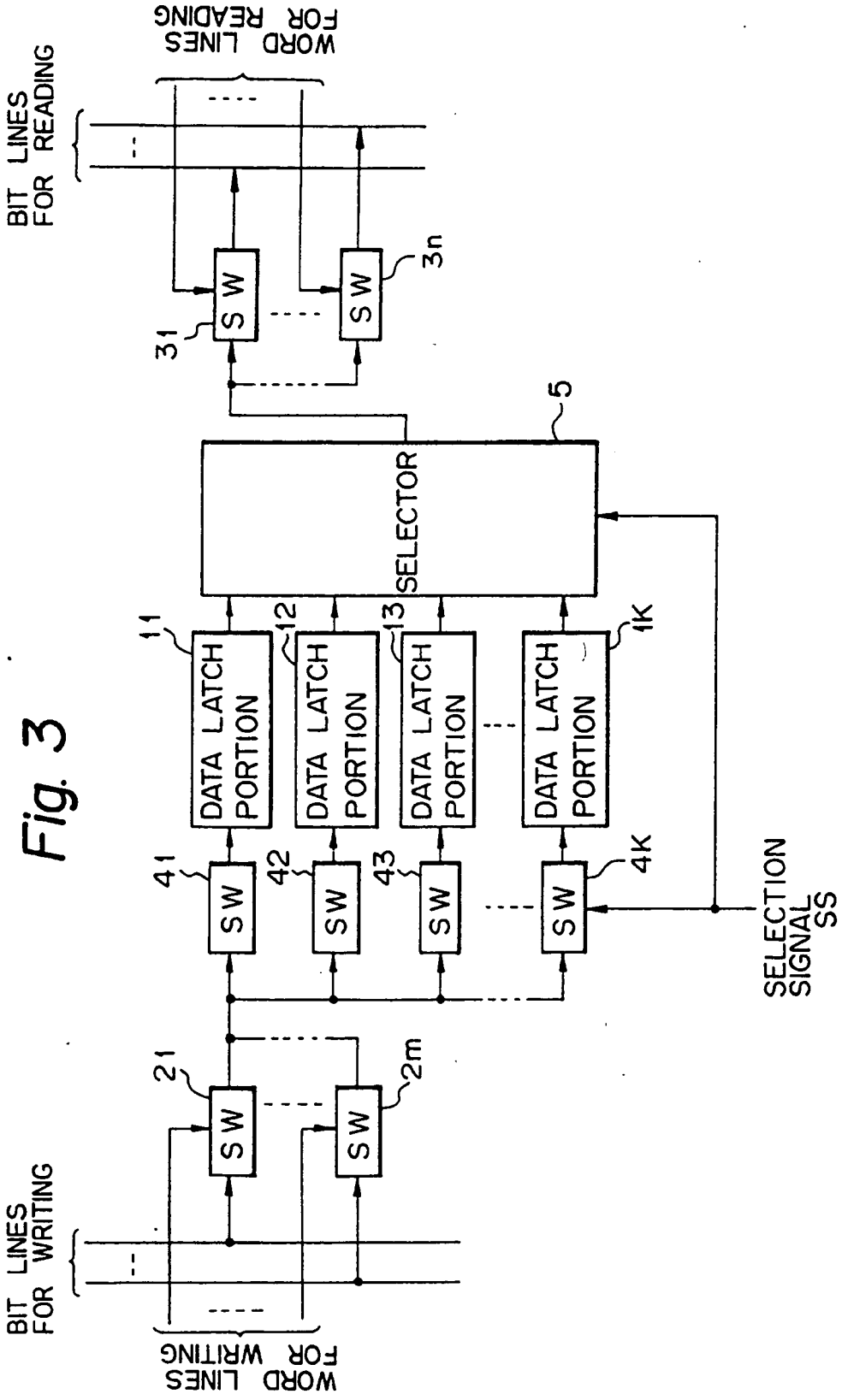
WORD LINES FOR READING
BIT LINES FOR READING
SW
31
3n
5
SELECTOR
DATA LATCH PORTION
11
12
13
1K
41
42
43
4K
SELECTION SIGNAL SS
21
2m
BIT LINES FOR WRITING
WORD LINES FOR WRITING

Fig. 4

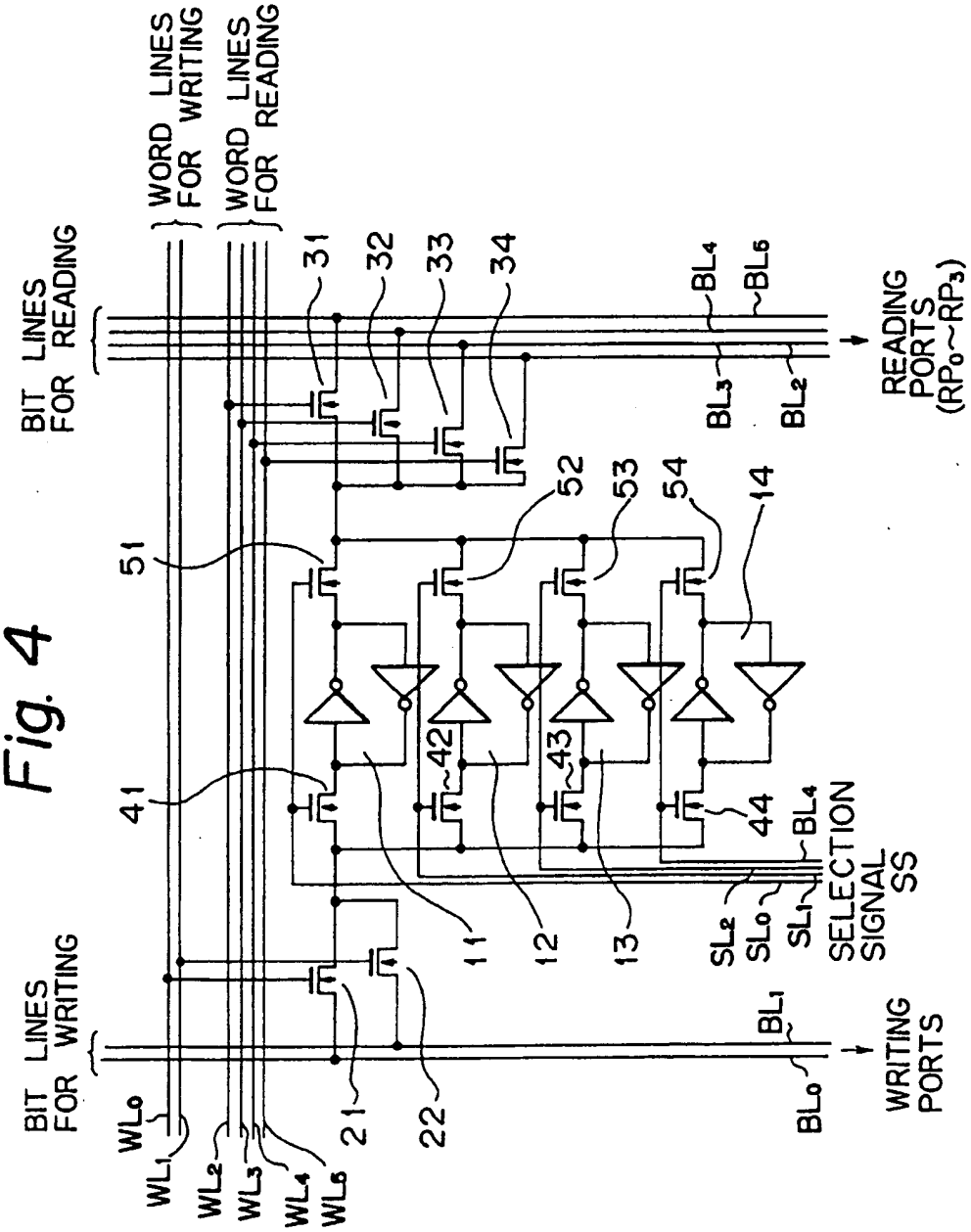
BIT LINES FOR READING
WORD LINES FOR WRITING
WORD LINES FOR READING
BIT LINES FOR WRITING
READING PORTS (RP0~RP3)
WRITING PORTS
SELECTION SIGNAL SS
WL0
WL1
WL2
WL3
WL4
WL5
BL0
BL1
BL2
BL3
BL4
BL5
SL0
SL1
SL2
11
12
13
14
21
22
31
32
33
34
41
42
43
44
51
52
53
54

Fig. 5

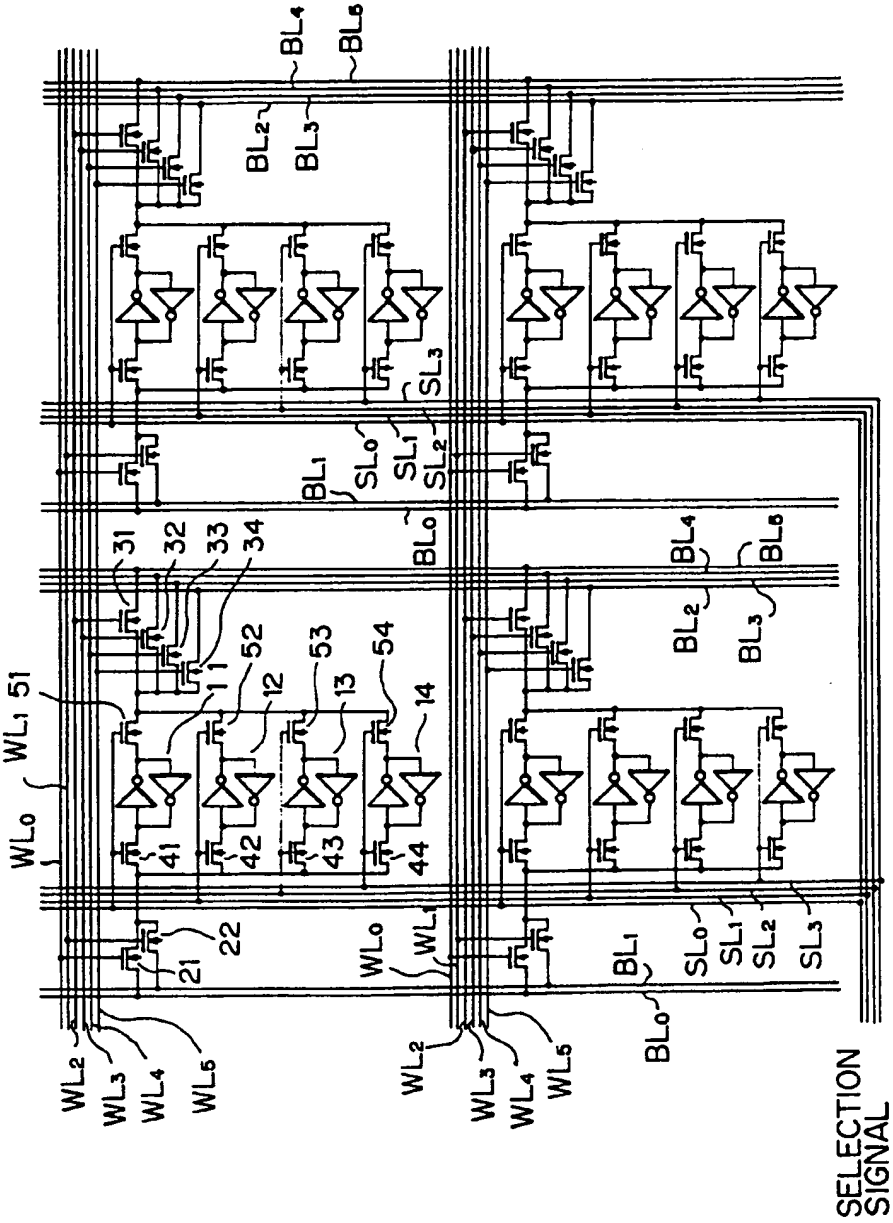
WL0
WL1
WL2
WL3
WL4
WL5
WL6
BL0
BL1
BL2
BL3
BL4
BL5
SL0
SL1
SL2
SL3
SELECTION SIGNAL
11
12
13
14
21
22
31
32
33
34
41
42
43
44
51
52
53
54

Fig. 6

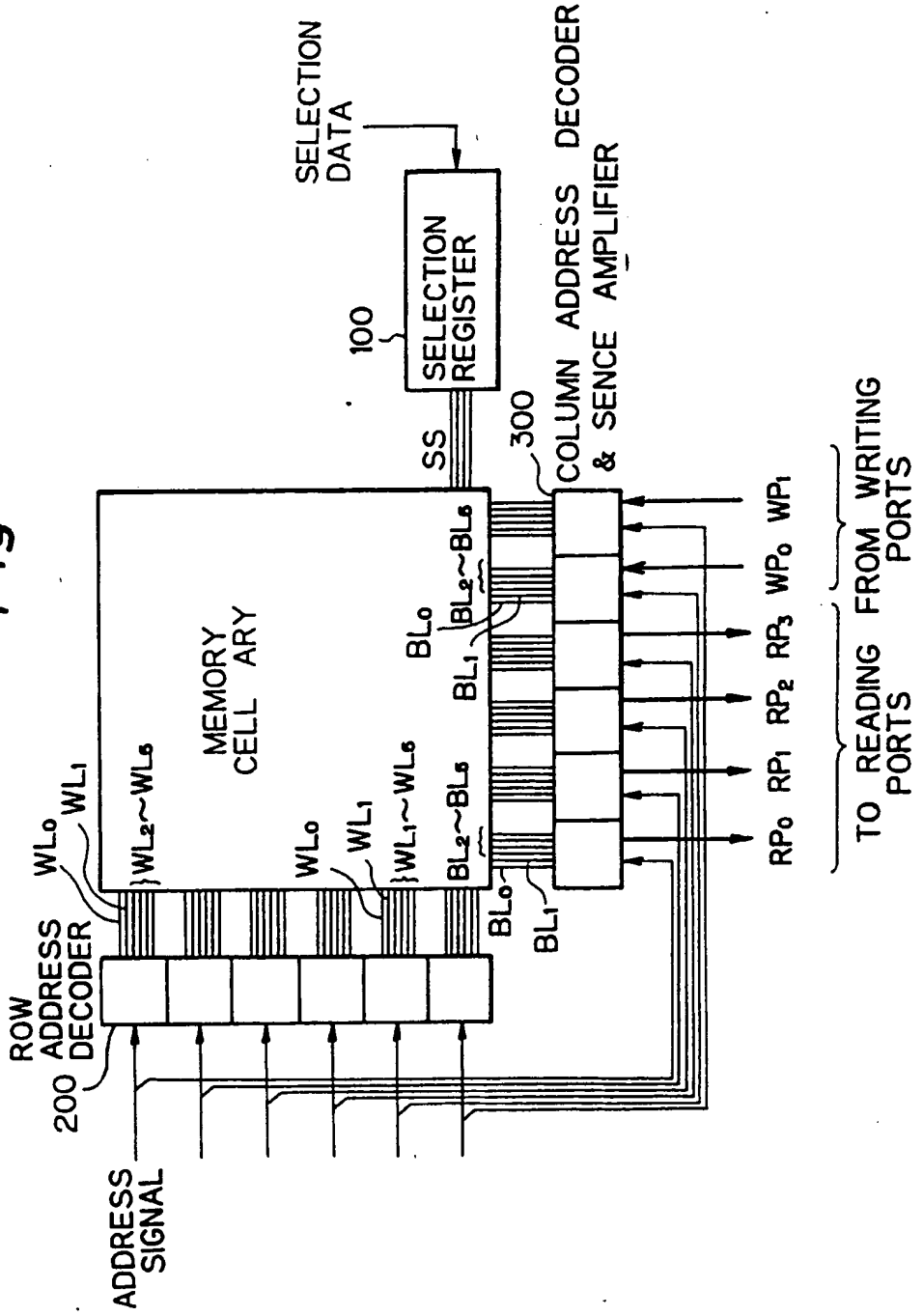
SELECTION DATA
100
SELECTION REGISTER
SS
300
COLUMN ADDRESS DECODER & SENCE AMPLIFIER
MEMORY CELL ARY
ROW ADDRESS DECODER
200
ADDRESS SIGNAL
WL0
WL1
WL2~WL6
WL1~WL6
BL0
BL1
BL2~BL6
RP0 RP1 RP2 RP3 WP0 WP1
TO READING PORTS
FROM WRITING PORTS

Fig. 7

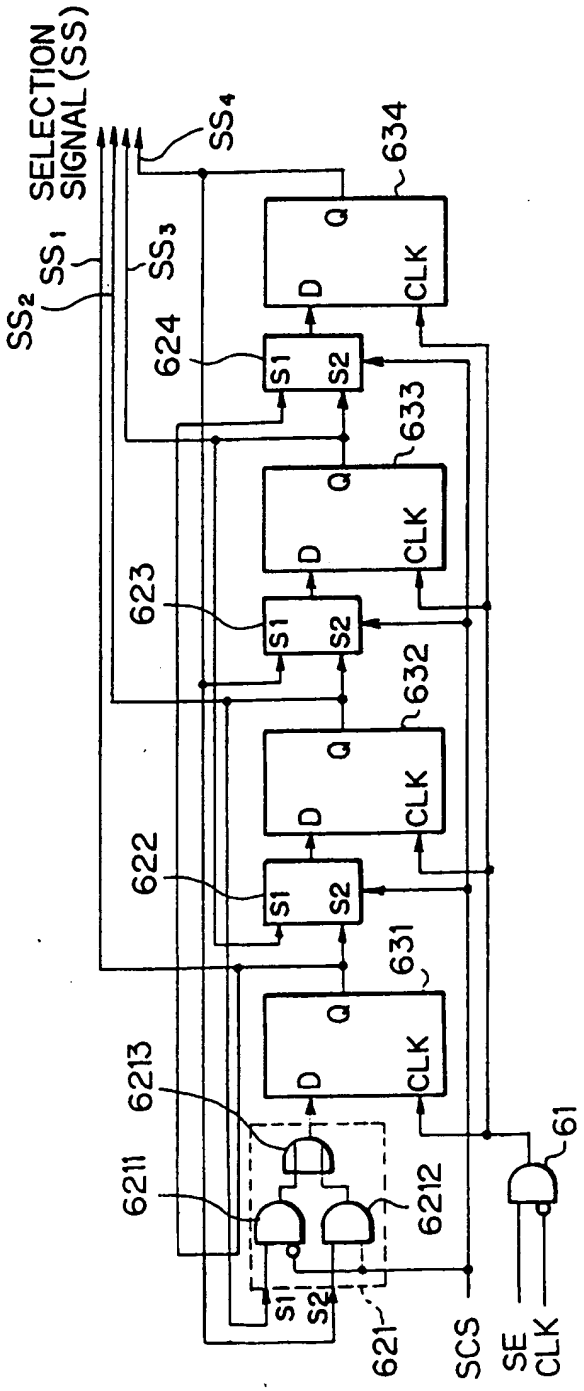
SELECTION SIGNAL (SS)
SS1
SS2
SS3
SS4
634
633
632
631
624
623
622
6213
6211
6212
621
61
D
Q
CLK
S1
S2
SCS
SE
CLK

Fig. 8

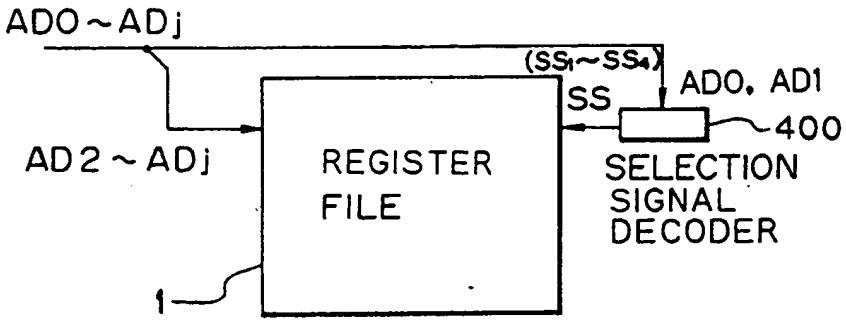
AD0~ADj
(SS1~SS4)
SS
AD0, AD1
400
AD2~ADj
REGISTER FILE
SELECTION SIGNAL DECODER
1

Fig. 9

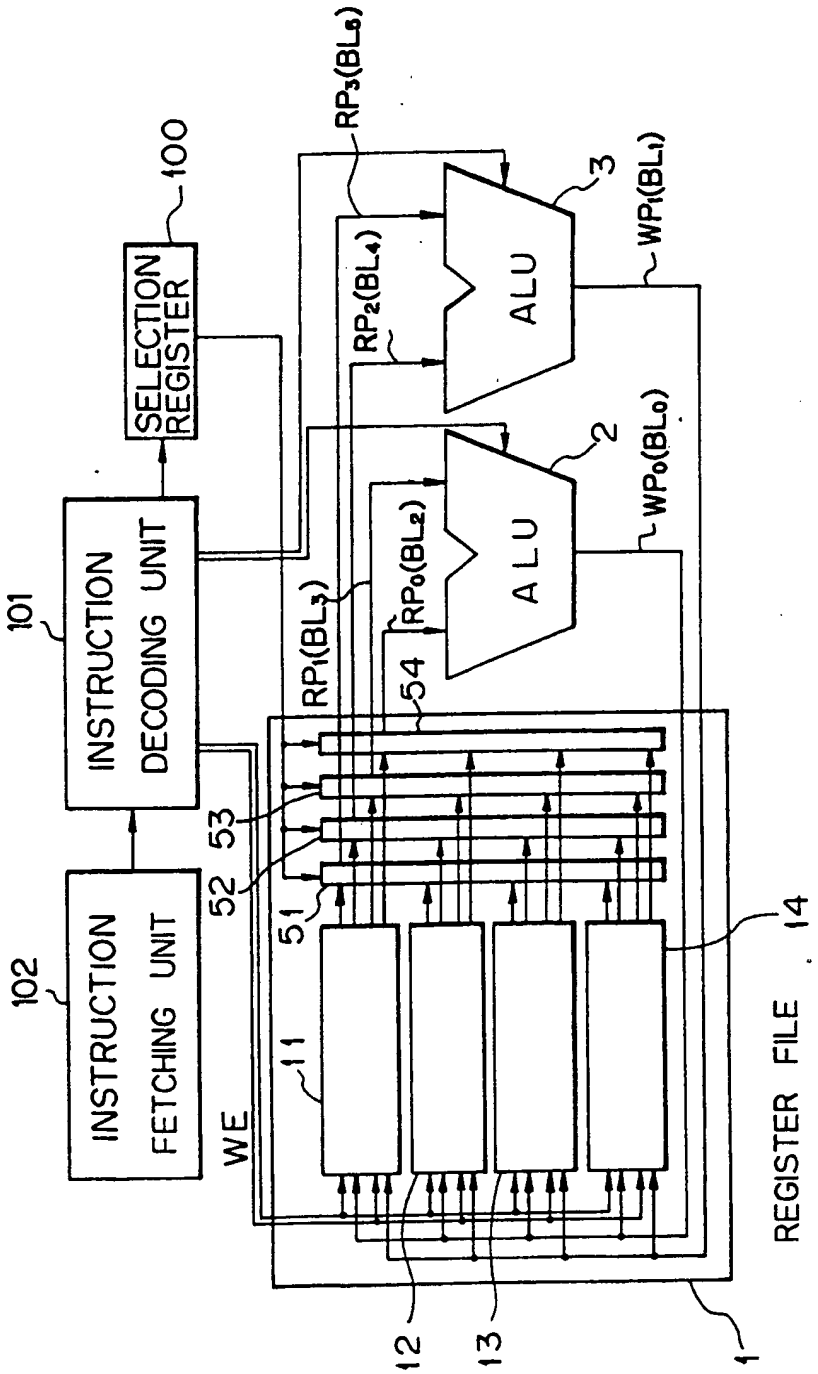
INSTRUCTION FETCHING UNIT
INSTRUCTION DECODING UNIT
SELECTION REGISTER
ALU
ALU
REGISTER FILE
WE
RP3(BL5)
RP2(BL4)
RP1(BL3)
RP0(BL2)
WP1(BL1)
WP0(BL0)
100
101
102
1
2
3
11
12
13
14
51
52
53
54

Fig. 10

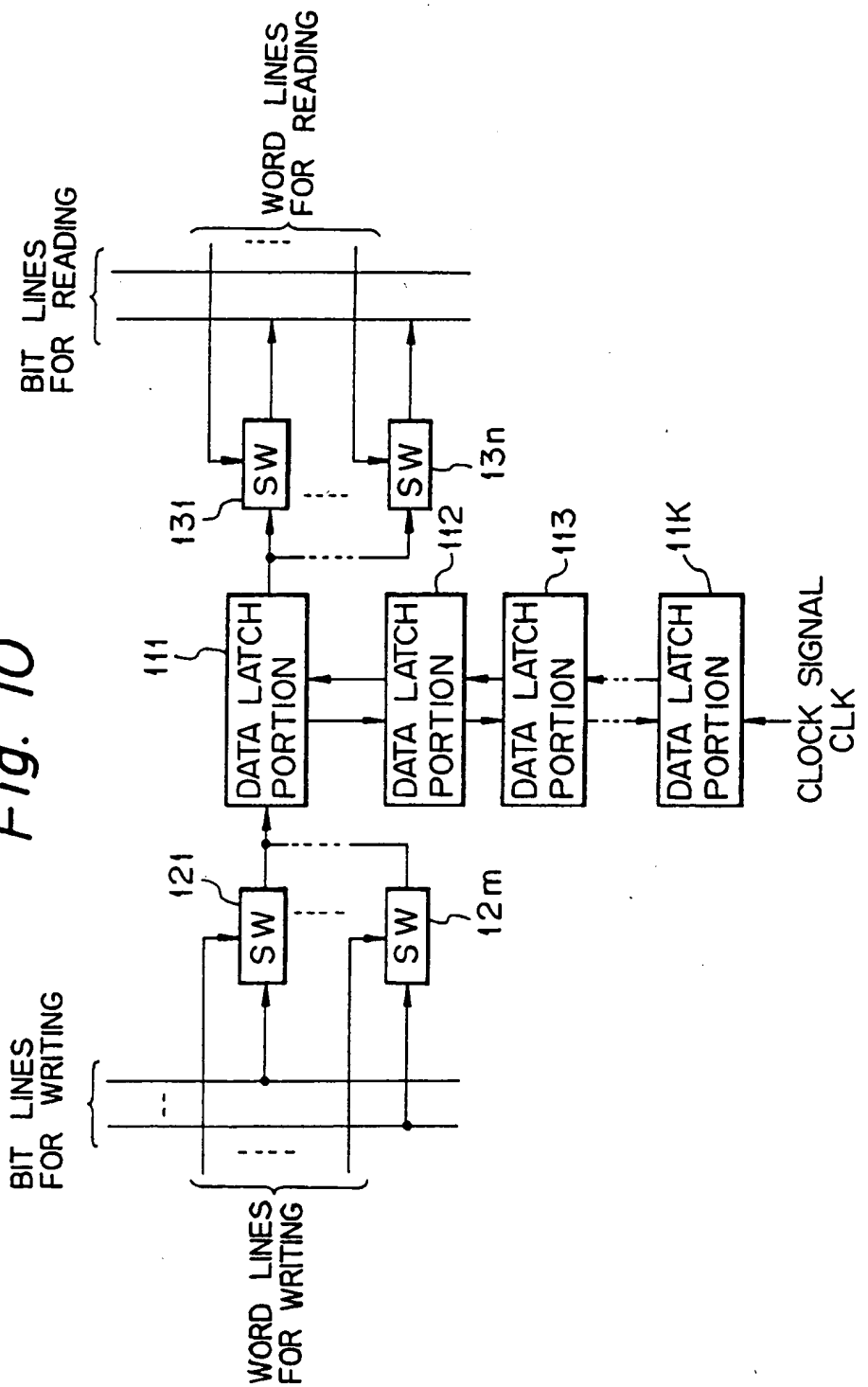
BIT LINES FOR READING
WORD LINES FOR READING
BIT LINES FOR WRITING
WORD LINES FOR WRITING
SW
131
13n
121
12m
111
112
113
11K
DATA LATCH PORTION
CLOCK SIGNAL CLK

Fig. 11A

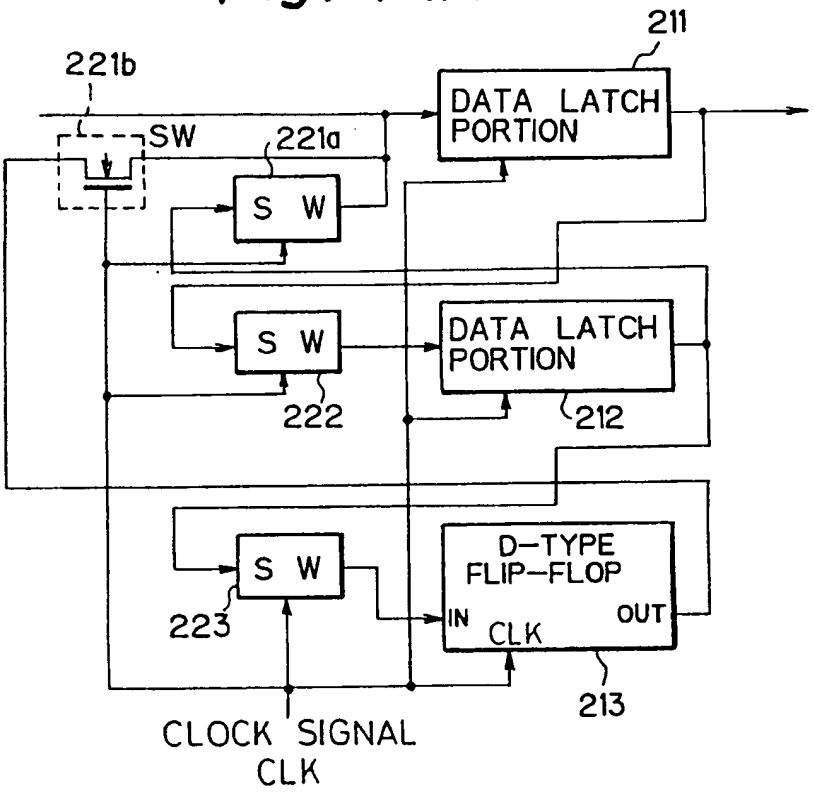

Fig. 11B